

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard C. Foss, Peter B. Gillingham, Robert Harland,
Masami Mitsuhashi and Atsusui Wada

Application No.: 10/032,431 Group: 2627

Filed: December 21, 2001 Examiner: Dinh, Tan X.

Confirmation No.: 8755

For: DYNAMIC RANDOM ACCESS MEMORY USING IMPERFECT
ISOLATING TRANSISTORS



CERTIFICATE OF MAILING OR TRANSMISSION	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:	
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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02/22/2007 EMAIL1 00000043 10032431

02 FC:1006

180.00 OP

Sir:

This Information Disclosure Statement is submitted under 37 C.F.R. 1.97(c) together with a \$180.00 fee, as required by 37 C.F.R. 1.17(p).

Applicant wishes to inform the Examiner that claims have been asserted against patents to which the instant application claims priority, as follows:

1. In *MOSAID Technologies, Inc. v. Infineon, et al.*, Civil Action No. 6:05-cv-00120, Eastern District of Texas, claims were asserted against U.S. Patent Nos. 5,414,662 and its reissue, RE37,641 (to which the instant application is a continuation). Status: Dismissed (See attached Order of Stipulated Dismissal with Prejudice).
2. In *Micron v. Mosaid, et al.*, Civil Action No. 06-04496, currently pending in the Northern District of California, claims have been asserted against U.S. Patent Nos. RE37,641 (to which the instant application is a continuation). Status: Appeal of Dismissal pending.

Previously uncited references cited by Defendant, Infineon, in its pleadings, are cited herein, although not all are considered to be prior art. Copies of the relevant pleadings citing those references are also included.

- ☒ Enclosed herewith is form PTO-1449:
- ☒ Copies of the cited references (C3 – C38) are enclosed.
- ☒ Copies of issued U.S. patents and published U.S. applications are not required and are not being provided.

It is requested that the information disclosed herein be made of record in this application.

Method of payment:

- ☒ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply. A copy of this Statement is enclosed.
- ☐ Please charge Deposit Account 08-0380 in the amount of \$[]. A copy of this Statement is enclosed.
- ☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

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Dated: 2/15/7

PTO-1449 REPRODUCED

**SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT
IN AN APPLICATION**

February 15, 2007

(Use several sheets if necessary)

ATTORNEY DOCKET NO.
2037.1002-003

APPLICATION NO.
10/032,431

FIRST NAMED INVENTOR
Richard C. Foss

FILING DATE
December 21, 2001

EXAMINER
Dinh, Tan X.

CONFIRMATION NO.
8755

GROUP
2627

U.S. PATENT DOCUMENTS

EXAM- INER INI- TIAL	REF. NO.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A36	2,255,232	09-09-1941	Stern
	A37	4,463,440	07-31-1984	Nishiura, <i>et al.</i>
	A38	4,638,182	01-20-1987	McAdams
	A39	4,795,985	01-03-1989	Gailbreath, Jr.
	A40	4,931,992	06-05-1990	Ogihara, <i>et al.</i>
	A41	4,994,688	02-19-1991	Horiguchi, <i>et al.</i>
	A42	5,029,136	07-02-1991	Tran, <i>et al.</i>
	A43	5,101,107	03-31-1992	Stoot
	A44	5,101,117	03-31-1992	Johnson, <i>et al.</i>
	A45	5,109,394	04-28-1992	Hjerpe, <i>et al.</i>
	A46	5,111,063	05-05-1992	Iwata
	A47	5,148,399	09-15-1992	Cho, <i>et al.</i>
	A48	5,220,206	06-15-1993	Tsang, <i>et al.</i>
	A49	5,252,867	10-12-1993	Sorrells, <i>et al.</i>
	A50	5,272,390	12-21-1993	Watson, Jr., <i>et al.</i>
	A51	5,295,164	03-15-1994	Yamamura
	A52	5,371,764	12-06-1994	Gillingham, <i>et al.</i>
	A53	5,384,735	01-24-1995	Park, <i>et al.</i>
	A54	5,412,615	05-02-1995	Noro, <i>et al.</i>
	A55	5,414,381	05-09-1995	Nelson, <i>et al.</i>

EXAMINER

DATE CONSIDERED

PTO-1449 REPRODUCED SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION February 15, 2007 (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.1002-003		APPLICATION NO. 10/032,431	
	FIRST NAMED INVENTOR Richard C. Foss		FILING DATE December 21, 2001	
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	A56	5,432,823	07-11-1995	Gasbarro, <i>et al.</i>
	A57	5,444,203	08-22-1995	Gunnarsson
	A58	5,463,337	10-31-1995	Leonowich
	A59	5,610,543	03-11-1997	Chang, <i>et al.</i>
	A60	5,657,481	08-12-1997	Farmwald, <i>et al.</i>
	A61	5,703,475	12-30-1997	Lee, <i>et al.</i>
	A62	5,734,292	03-31-1998	Shirai, <i>et al.</i>
	A63	5,777,501	07-07-1998	AbouSeido
	A64	5,812,832	09-22-1998	Horne, <i>et al.</i>
	A65	5,880,624	03-09-1999	Koyanagi, <i>et al.</i>
	A66	5,991,226	11-23-1999	Bhullar
	A67	6,067,592	05-23-2000	Farmwald, <i>et al.</i>
	A68	6,087,868	07-11-2000	Millar
	A69	6,314,052	11-06-2001	Foss, <i>et al.</i>
	A70	6,327,318	12-04-2001	Bhullar, <i>et al.</i>
	A71	6,510,503	01-21-2003	Gillingham, <i>et al.</i>
	A72	6,657,918	12-02-2003	Foss, <i>et al.</i>

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
C3	1992 Xerox Presentation re. use of on-chip DLL	
C4	Adler, E., "The Evolution of IBM CMOS DRAM Technology," <i>IBM J. Res. Develop.</i> , Vol. 39 No. 1/2, January/March 1995, p. 169.	
C5	Anceau, "A Synchronous Approach for Clocking VLSI Systems," <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-17, No. 1 (Feb. 1982).	
C6	Chen, "Designing On-Chip Clock Generators," <i>Circuits and Devices</i> , July, 1992, pp. 32-36.	
C7	Chou, Shizuo, <i>et al.</i> , "A 60-ns 16M-bit DRAM With a Minimized Sensing Delay Caused by Bit-Line Stray Capacitance," <i>IEEE Journal of Solid State Circuits</i> , Vol. 24, No. 5, Oct. 1989, pp. 1176-1178.	
C8	Foss, R.C., <i>et al.</i> , "Application of a High-Voltage Pumped Supply for Low-Power DRAM," <i>IEEE 1992 Symposium on VLSI Circuits Digest of Technical Papers</i> , pp. 106-07.	
C9	Fujii, Syuso, <i>et al.</i> , "A 45-ns 16-Mbit DRAM with Triple-Well Structure," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 5, October 1989, pp. 1170-1174	
C10	Gasbarro, <i>et al.</i> , "Techniques for Characterizing DRAMS With a 500 MHz Interface," International Test Conference, Oct. 1994, pp. 516-525.	
C11	Gasbarro, "Testing High Speed DRAMS," International Test Conference, Oct. 1994, p. 361.	
C12	Gillingham, Peter, <i>et al.</i> , "High-Speed, High-Reliability Circuit Design for Megabit DRAM," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 26, No. 8, August 1991, pp. 1171-1175	
C13	Horowitz, Mark, "Clocking Strategies in High Performance Processors," <i>1992 Symposium on VLSI Circuits Digest of Technical Papers</i> , pp. 50-53.	
C14	Horowitz, M., <i>et al.</i> , "PLL Design for a 500 MB/s Interface," <i>ISSCC Digest of Technical Papers</i> (Feb. 1993)	
C15	Johnson, <i>et al.</i> , "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 23, No. 5, October, 1988, pp. 1218-1223.	
C16	Kim, S., <i>et al.</i> , "A Pseudo-Synchronous Skew-Insensitive I/O Scheme for High Bandwidth Memories," <i>1994 Symposium on VLSI Circuits Digest of Technical Papers</i> , pp. 41-42.	
C17	Menasce, V., <i>et al.</i> , "A Fully Digital Phase Locked Loop," Canadian Conference on VLSI, Oct. 1990, pp. 9.4.1 – 9.4.8.	
C18	NEC, PLL Enable Mode, JC-42.3 (Sept. 14, 1994) (FIN 023321 – 023377).	

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	EXAMINER Dinh, Tan X.	CONFIRMATION NO. 8755	GROUP 2627

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

C19	Patent Application for Delay Locked Loop (DLL) Implementation in a Synchronous Dynamic Random Access Memory, Sep. 29, 1994 (MTI0000118755 – 118768).
C20	Przybylski, Steven, <u>New DRAM Technologies, A Comprehensive Analysis of the New Architectures</u> , MicroDesign Resources, Sebastopol, CA, (1994).
C21	Rambus document RM 2744932-33, details Rambus making certain technical information publicly available on the internet in November 1993.
C22	Rambus Product Catalog, by Rambus, Inc., 1993.
C23	RDRAM Reference Manual, by Rambus, Inc., 1993.
C24	Schanke, Morten, "Proposal for Clock Distribution in SCI," May 5, 1989.
C25	Sidiropoulos, Stefanos, <i>et al.</i> , "A CMOS 500 Mbps/pin synchronous point to point link interface," <i>1994 Symposium on VLSI Circuits, Digest of Technical Papers</i> , pp. 43-44.
C26	Wagner, Kenneth, <i>et al.</i> , "Testable Programmable Digital Clock Pulse Control Elements," <i>International Test Conference 1993</i> , pp. 902 – 909.
C27	Waizman, Alex, "A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," <i>1994 IEEE Solid State Circuits Conference</i> , pp. 298-299.
C28	Deposition of Thomas Vogelsang, dated 6/4/04.
C29	MOSAID's Complaint for Patent Infringement and Jury Demand, filed 4/6/05, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
C30	Defendants' [Infineons'] Answer and Counterclaims, filed 6/15/05, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
C31	MOSAID's Reply to Infineon's Counterclaims, filed 6/29/05, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
C32	Infineon's Preliminary Invalidity Contentions Pursuant to Local Patent Rule 3-3, filed 1/31/06, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
C33	Infineon's Amended Preliminary Invalidity Contentions Pursuant to Local Patent Rule 3-3, served 2/7/06, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
	C34	[MOSAID's] First Amended Complaint for Patent Infringement and Jury Demand, filed 3/30/06, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
	C35	[MOSAID's] Second Amended Complaint for Patent Infringement, filed 4/20/06, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
	C36	[Infineons'] Answer and Counterclaims to Second Amended Complaint, filed 5/4/06, <i>Mosaid Technologies, Inc. v. Infineon North America Corp., et al</i> , Civil Action No. 05-00120 (E. D. TX).
	C37	Micron's Complaint for Declaratory Judgment, filed 7/24/06, <i>Micron Technology, Inc. v. Mosaid Technologies, Incorporated</i> , Civil Action No. 06-04496 (N.D.CA).
	C38	Order Granting Mosaid's Motion to Dismiss for Lack of Subject Matter Jurisdiction, entered 10/23/06, <i>Micron Technology, Inc. v. Mosaid Technologies, Incorporated</i> , Civil Action No. 06-04496 (N.D.CA).

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